What the invention claimed is:

1. A logic analyzer data processing method used in a logic analyzer, which comprises a control circuit adapted to read in test data from a test sample, a memory controlled by said control circuit to store the test data received from said test sample, and display means adapted to display the test data fetched by said control circuit from said memory, the method comprising the step of enabling said control circuit to drive a compressor to compress the test data received from said test sample before storing the test data in said memory.

2. The logic analyzer data processing method as claimed in claim 1, wherein said test sample is digital circuit.

3. The logic analyzer data processing method as claimed in claim 2, wherein the test data from said test sample includes high/low potential status of every pin of said test sample at a fixed time internal.

4. A logic analyzer data processing method used in a logic analyzer, which comprises a control circuit adapted to read in test data from a test sample, a memory controlled by said control circuit to store the test data received from said test sample, and display means adapted to display the test data fetched by said control circuit from said memory, the method comprising the step of enabling said control circuit to drive a compressor to compress the

test data received from said test sample before storing the test sample in said memory, and to depress the compressed test data before transmitting from said memory to said display means.

5. The logic analyzer data processing method as claimed in claim 4, wherein said test sample is a digital circuit.

6. The logic analyzer data processing method as claimed in claim 5, wherein the test data from said test sample includes high/low potential status of every pin of said test sample at a fixed time internal.